IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: WANG *et al.* Appl. No.: To Be Assigned *(Continuation of Appl. No. 10/151,932; Filed: May 22, 2002)* Filed: April 2, 2004 For: **System And Method For Retiring Approximately Simultaneously A Group Of Instructions In A Superscalar Microprocessor**	Confirmation No.: To Be Assigned Art Unit: To Be Assigned Examiner: To Be Assigned Atty. Docket: SP038.C5 (1397.0140005)

Information Disclosure Statement

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Where the publication date of a listed document does not provide a month of publication, the year of publication of the listed document is sufficiently earlier than the effective U.S. filing date and any foreign priority date so that the month of publication is not in issue. Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may

not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 C.F.R. § 1.56(c) more than thirty days prior to the filing of this information disclosure statement.

☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being **filed within three months of the date of filing of a national application** other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of $_____ in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee.

Enclosed find our PTO-2038 Credit Card Payment Form in the amount of $_____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.

☐ 6. A concise explanation of the relevance of the non-English language document(s) appears below:

☐ 7. Copies of the documents are submitted herewith.

☒ 8. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No.10/151,932, filed May 22, 2002, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Thomas C. Fiala
Attorney for Applicants
Registration No. 43,610

Date: April 2, 2004

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Washington, D.C. 20005-3934
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FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
SP038.C5 (1397.0140005)	To Be Assigned
FIRST NAMED INVENTOR	
WANG et al.	
FILING DATE	ART UNIT
April 2, 2004	To Be Assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	4,626,989	12/02/1986	Torii			
	AB1	4,675,806	06/23/1987	Uchida			
	AC1	4,722,049	01/26/1988	Lahti			
	AD1	4,807,115	02/21/1989	Torng			
	AE1	4,823,201	04/18/1989	Simon et al.			
	AF1	4,903,196	02/20/1990	Pomerene et al.			
	AG1	4,942,525	07/17/1990	Shintani et al.			
	AH1	5,067,069	11/19/1991	Fite et al.			
	AI1	5,072,364	12/10/1991	Jardine et al.			
	AJ1	5,109,495	04/28/1992	Fite et al.			
	AK1	5,125,083	06/23/1992	Fite et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1	WO 88/09035	11/1988	PCT			Yes No
	AM1	0 515 166	11/1992	EP			Yes No
	AN1	H2-48732	02/19/1990	Japan			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AO	1	Acosta, R. D. *et al.*, "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors," *IEEE Transactions On Computers*, IEEE, Vol. C-35, No. 9, pp. 815-828 (September 1986).
	AP	1	Agerwala, T. and Cocke, J., "High Performance Reduced Instruction Set Processors," IBM Research Division, pp. 1-61 (March 31, 1987).
	AR	1	Butler, M. and Patt, Y., "An Improved Area-Efficient Register Alias Table for Implementing HPS," University of Michigan, Ann Arbor, Michigan, 24 pages (January 1990).
	AS	1	Butler, M. *et al.*, "Single Instruction Stream Parallelism Is Greater than Two," *Proceedings of the 18th Annual International Symposium on Computer Architecture*, ACM, pp. 276-286 (May 1991).
	AT	1	Charlesworth, A.E., "An Approach to Scientific Array Processing: The Architectural Design of the AP-120B/FPS-164 Family," *Computer*, IEEE, Vol. 14, pp. 18-27 (September 1981).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2	5,148,536	09/15/1992	Witek et al.			
	AB2	5,167,026	11/24/1992	Murray et al.			
	AC2	5,179,673	01/12/1993	Steely, Jr. et al.			
	AD2	5,197,132	03/23/1993	Steely, Jr. et al.			
	AE2	5,214,763	03/25/1993	Blaner et al.			
	AF2	5,222,240	06/22/1993	Patel			
	AG2	5,226,126	07/06/1993	McFarland et al.			
	AH2	5,230,068	07/20/1993	Van Dyke et al.			
	AI2	5,251,306	10/05/1993	Tran			
	AJ2	5,317,720	05/31/1994	Stamm et al.			
	AK2	5,345,569	09/06/01994	Tran			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL2	H4-96132	03/27/1992	Japan			Yes No
	AM2	H6-19707	01/28/1994	Japan			Yes No
	AN2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AO	2	Colwell, R.P. *et al.*, "A VLIW Architecture for a Trace Scheduling Compiler," *Proceedings of the 2nd International Conference on Architectural Support for Programming Languages and Operating Systems*, ACM, pp. 180-192 (October 1987).
	AP	2	Dwyer, H, *A Multiple, Out-of-Order Instruction Issuing System for Superscalar Processors*, UMI, pp. 1-249 (August 1991).
	AR	2	Foster, C.C. and Riseman, E.M., "Percolation of Code to Enhance Parallel Dispatching and Execution," *IEEE Transactions On Computers*, IEEE, pp. 1411-1415 (December 1971).
	AS	2	Gee, J. *et al.*, "The Implementation of Prolog via VAX 8600 Microcode," *Proceedings of Micro 19*, IEEE, October 1986, pp.68-74.
	AT	2	Gross, T.R. and Hennessy, J.L., "Optimizing Delayed Branches," *Proceedings of the 5th Annual Workshop on Microprogramming*, IEEE, pp. 114-120 (October 5-7, 1982).

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA3	5,355,457	10/11/1994	Shebanow et al.			
	AB3	5,367,660	11/22/1994	Gat et al.			
	AC3	5,390,355	02/14/1995	Horst			
	AD3	5,398,330	03/14/1995	Johnson			
	AE3	5,430,888	07/04/1995	Witek et al.			
	AF3	5,442,757	08/15/1995	McFarland et al.			
	AG3	5,487,156	01/23/1996	Popescu et al.			
	AH3	5,560,032	09/24/1996	Nguyen et al.			
	AI3	5,561,776	10/01/1996	Popescu et al.			
	AJ3	5.568,624	10/22/1996	Sites et al.			
	AK3	5,574,927	11/12/1996	Scantlin			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL3						Yes No
	AM3						Yes No
	AN3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AO	3	Hennessy, J.L. and Patterson, D.A., *Computer Architecture: A Quantitative Approach*, Morgan Kaufmann Publishers, pp. xi-xv, 257-278, 290-314 and 449 (1990).
	AP	3	Hwu, W-M. W. and Patt, Y.N., "Checkpoint Repair for High-Performance Out-of-Order Execution Machines," *IEEE Trans. On Computers*, IEEE, Vol. C-36, No. 12, pp. 1496-1514 (December 1987).
	AR	3	Hwu, W. and Patt, Y., "Design Choices for the HPSm Microprocessor Chip," *Proceedings of the Twentieth Annual Hawaii International Conference on System Sciences*, pp. 330-336 (1987).
	AS	3	Hwu, W-M. W. and Chang, P.P., "Exploiting Parallel Microprocessor Microarchitectures with a Compiler Code Generator," *Proceedings of the 15th Annual Symposium on Computer Architecture*, IEEE, pp. 45-53 (June 1988).
	AT	3	Hwu, W-M. *et al.*, "An HPS Implementation of VAX: Initial Design and Analysis," *Proceedings of the Nineteenth Annual Hawaii International Conference on System Sciences*, pp. 282-291 (1986).

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4	5,592,636	01/07/1997	Popescu et al.			
	AB4	5,625,837	04/29/1997	Popescu et al.			
	AC4	5,627,983	05/06/1997	Popescu et al.			
	AD4	5,630,149	05/13/1997	Bluhm			
	AE4	5,651,125	07/22/1997	Witt et al.			
	AF4	5,708,841	01/13/1998	Popescu et al.			
	AG4	5,768,575	06/16/1998	McFarland et al.			
	AH4	5,778,210	07/07/1998	Henstrom et al.			
	AI4	5,797,025	08/18/1998	Popescu et al.			
	AJ4	5,826,055	10/20/1998	Wang et al.			
	AK4	5,832,205	11/03/1998	Kelly et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL4						Yes No
	AM4						Yes No
	AN4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AO	4	Hwu, W-M. and Patt, Y.N., "HPSm, a High Performance Restricted Data Flow Architecture Having Minimal Functionality," *Proceedings from ISCA-13*, IEEE, pp. 297-306 (June 2-5, 1986).
	AP	4	Hwu, W. and Patt, Y., "HPSm2: A Refined Single-Chip Microengine," *HICSS '88*, IEEE,pp. 30-40 (1988).
	AR	4	*IBM Journal of Research and Development*, IBM, Vol. 34, No. 1, pp. 1-70 (January 1990).
	AS	4	Johnson, M. *Superscalar Microprocessor Design*, Prentice-Hall, pp. vii-xi and 87-125 (1991).
	AT	4	Johnson, W. M., *Super-Scalar Processor Design*, (Dissertation), 134 pages (1989).

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA5	5,832,293	11/03/1998	Popescu et al.			
	AB5	6,131,157	10/10/2000	Wang et al.			
	AC5	6,412,064	06/25/2002	Wang et al.			
	AD5	5,961,629	10/05/1999	Nguyen et al.			
	AE5						
	AF5						
	AG5						
	AH5						
	AI5						
	AJ5						
	AK5						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL5						Yes No
	AM5						Yes No
	AN5						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AO	5	Jouppi, N.P. and Wall, D.W., "Available Instruction-Level Parallelism for Superscalar and Superpipelined Machines," *Proceedings of the 3rd International Conference on Architectural Support for Programming Languages and Operating Systems*, ACM, pp. 272-282 (April 1989).
	AP	5	Keller, R.M., "Look-Ahead Processors," *Computing Surveys*, ACM, Vol. 7, No. 4, pp. 177-195 (December 1975).
	AR	5	Lightner, B.D. and Hill, G., "The Metaflow Lightning Chipset", *Compcon Spring 91*, IEEE, pp. 13-18 (February 25 - March 1, 1991).
	AS	5	Patt, Y.N. *et al.*, "Critical Issues Regarding HPS, A High Performance Microarchitecture", *Proceedings of 18th Annual Workshop on Microprogramming*, IEEE, pp. 109-116 (December 3-6, 1985).
	AT	5	Hwu *et al.*, "Experiments with HPS, a Restricted Data Flow Microarchitecture for High Performance Computers," *COMPCON 86*, IEEE, pp. 254-258 (1986).

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA6						
	AB6						
	AC6						
	AD6						
	AE3						
	AF6						
	AG6						
	AH6						
	AI6						
	AJ6						
	AK6						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL6						Yes No
	AM6						Yes No
	AN6						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AO	6	Patt, Y.N. *et al.*, "HPS, A New Microarchitecture: Rationale and Introduction", *The 18th Annual Workshop on Microprogramming*, Pacific Grove, CA, December 3-6, 1985, IEEE Computer Society Order No. 653, pp. 103-108.
	AP	6	Patt *et al.*, "Run-Time Generation of HPS Microinstructions From a VAX Instruction Stream," *Proceedings of MICRO 19 Workshop*, New York, pp. 75-81 (October 1986).
	AR	6	Peleg, A. and Weiser, U., "Future Trends in Microprocessors: Out-of-Order Execution, Speculative Branching and their CISC Performance Potential", IEEE, pp. 263-266 (1991).
	AS	6	Pleszkun, A.R. and Sohi, G.S., "The Performance Potential of Multiple Functional Unit Processors," *Proceedings of the 15th Annual Symposium on Computer Architecture*, IEEE, pp. 37-44 (June 1988).
	AT	6	Pleszkun, A.R. *et al.*, "WISQ: A Restartable Architecture Using Queues," *Proceedings of the 14th International Symposium on Computer Architecture*, ACM, pp. 290-299 (June 1987).

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA7						
	AB7						
	AC7						
	AD7						
	AE7						
	AF7						
	AG7						
	AH7						
	AI7						
	AJ7						
	AK7						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL7						Yes No
	AM7						Yes No
	AN7						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AO	7	Popescu, V. *et al.*, "The Metaflow Architecture", *IEEE Micro*, IEEE, Vol. 11, No.3, pp. 10-13 and 63-73 (June 1991).
	AP	7	Smith, J.E. and Pleszkun, A.R., "Implementation of Precise Interrupts in Pipelined Processors," *Proceedings of the 12th Annual International Symposium on Computer Architecture*, IEEE, pp. 36-44 (June 1985).
	AR	7	Smith, M.D. *et al.*, "Limits on Multiple Instruction Issue," *Computer Architecture News*, ACM, No. 2, pp. 290-302 (April 3-6, 1989).
	AS	7	Sohi, G.S. and Vajapeyam, G.S., "Instruction Issue Logic For High-Performance, Interruptable Pipelined Processors," *Conference Proceedings of the 14th Annual International Symposium on Computer Architecture*, pp. 27-34 (June 2-5, 1987).
	AT	7	Thornton, J.E., *Design of a Computer: The Control Data 6600*, Control Data Corporation, pp. 57-140 (1970).

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	AA8						
	AB8						
	AC8						
	AD8						
	AE8						
	AF8						
	AG8						
	AH8						
	AI8						
	AJ8						
	AK3						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL8						Yes No
	AM8						Yes No
	AN8						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AO	8	Tjaden, G.S. and Flynn, M.J., "Detection and Parallel Execution of Independent Instructions," *IEEE Trans. On Computers*, IEEE, Vol. C-19, No. 10, pp. 889-895 (October 1970).
	AP	8	Tjaden, G.S., *Representation and Detection of Concurrency Using Ordering Matrices*, (Dissertation), UMI, pp. 1-199 (1972).
	AR	8	Tjaden *et al.*, "Representation of Concurrency with Ordering Matrices," *IEEE Transactions On Computers*, IEEE, Vol. C-22, No. 8, pp. 752-761 (August 1973).
	AS	8	Tomasulo, R.M., "An Efficient Algorithm for Exploiting Multiple Arithmetic Units," *IBM Journal*, IBM, Vol. 11, pp. 25-33 (January 1967).
	AT	8	Uht, A.K., "An Efficient Hardware Algorithm to Extract Concurrency From General-Purpose Code," *Proceedings of the 19th Annual Hawaii International Conference on System Sciences*, HICSS, pp. 41-50 (1986).

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	AA9						
	AB9						
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	AF9						
	AG9						
	AH9						
	AI9						
	AJ9						
	AK9						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL9						Yes No
	AM9						Yes No
	AN9						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AO	9	Uvieghara, G.A. *et al.*, "An Experimental Single-Chip Data Flow CPU," *Symposium on ULSI Circuits Design Digest of Technical Papers*, 2 pages (May 1990).
	AP	9	Uvieghara, G.A. *et al.*, "An Experimental Single-Chip Data Flow CPU," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 27, No. 1, pp. 17-28 (January 1992).
	AR	9	Wedig, R.G., *Detection of Concurrency In Directly Executed Language Instruction Streams*, (Dissertation), UMI, pp. 1-179 (June 1982).
	AS	9	Weiss, S. and Smith, J.E., "Instruction Issue Logic in Pipelined Supercomputers," *IEEE Trans. on Computers*, IEEE, Vol. C-33, No. 11, pp. 77-86 (November 1984).
	AT	9	Wilson, J.E. *et al.*, "On Tuning the Microarchitecture of an HPS Implementation of the VAX," *Proceedings of the 20th Annual Workshop on Microprogramming*, IEEE Computer Society, pp. 162-167 (December 1-4, 1987).

EXAMINER	DATE CONSIDERED

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. SP038.C5 (1397.0140005)	APPLICATION NO. To Be Assigned
	FIRST NAMED INVENTOR WANG et al.	
	FILING DATE April 2, 2004	ART UNIT To Be Assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA10						
	AB10						
	AC10						
	AD10						
	AE10						
	AF10						
	AG10						
	AH10						
	AI10						
	AJ10						
	AK10						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL10						Yes No
	AM10						Yes No
	AN10						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AO	10	Notice of Reasons For Rejection, dated November 5, 2003, issued in Japanese Patent Application No. H5-519128 (3 pages) with English translation (4 pages)
	AP	10	
	AR	10	
	AS	10	
	AT	10	

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